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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,771	12/30/2003	James Shyu	07942.0031-00	1047

22852 7590 05/10/2005

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,771	SHYU ET AL.	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 20 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend:

In independent claim 17, the "dielectric layer" is "formed *up to a level above the collar,*" yet in depending claim 20, the "dielectric layer" is "formed *up to a top level* of the collar," which does not further limit "up to a level above" since when the "level" is "above" the top of the collar, the "level" must also necessarily be "up to" the top as well. If claim 20 were considered as further limiting, the claim would contradict the previous claim 17, since when the level is "above the top" it could not then be "exactly at the top." Correction is required.

Specification

2. The specification is objected to for a lack of adequate explanation of how the transition from Fig. 2D to Fig. 2E is performed in accordance with the claimed invention, the transition from Fig. 2D to Fig. 2E being an essential part of enablement of the claim phrases: "the second insulating layer *being separated* from the first insulating layer *by an intermediate region*" (i.e. claims 1-11) and "forming a first insulating layer *up to a lower level* of the intermediate region...and forming a second insulating layer *down to an upper level* of the *intermediate region*" (i.e. claims 13-16).

The practice of claims 1-11 and 13-16 requires practice of the transition from Fig. 2D to 2E, without undue experimentation. Figs 2D and 2E are repeated here for clarity:

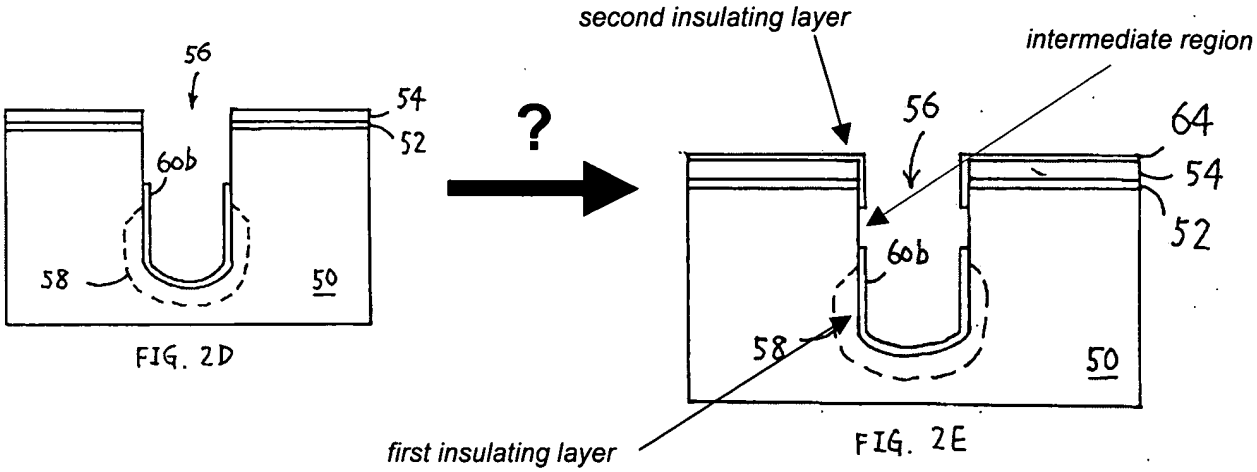

FIG. 2D

FIG. 2E

The written description for enablement of the claim phrases identified above consists of a single "example" as being an "ALD" process to form layer 64 (at p. 7, [026]), such that the layer is controlled to extend only part way down the trench 56 sidewalls, as depicted in Fig. 2E.

That is, ALD is used to form layer 64 with a "separation" seen as a gap between the "first and second insulating layers" at the "intermediate region" (claims 5, 10 & 15).

Yet, applicant does not explain how an ALD process is used to form layer 64 as depicted in Fig. 2E (as is claimed) because ALD is known to be a "conformal" process:

For example, Gutsche et al. explain that "trench capacitors require extremely conformal deposition techniques. Atomic Layer Deposition (ALD) was utilized to achieve superb step coverage..." [upper left of p. 18.6.2].

As another example, Senaki et al. explain that "Atomic Layer Deposition (ALD) has gained acceptance as a thin film deposition technique due to...step coverage over aggressive advanced IC device structures" [abstract].

That is, in the prior art, ALD would not readily be utilized to deposit a layer like 64 in Fig. 2E, without further instruction of how to use ALD *contrary* to its well-known benefits [i.e. applicant doesn't explain how applicant is using ALD for selective deposition on trench sidewalls rather than for conformal deposition over a contiguous surface inside the trench].

Correction and/or explanation are required.

Claim Rejections - 35 USC § 112

3. Claims 1-11 and 13-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to make the invention:

Claims 1-11 require enablement of forming an "intermediate region" that "separates" the "first and second insulating layers," in the context of trench capacitor sidewalls, while claims13-16 also require forming to get separation by the "intermediate region" because the "first layer" extends *up to* a "lower level" while the "second layer" extends *down to* an "upper level" of the "intermediate region."

Particularly rejected claims 5, 10 and 15 are puzzling in view of evidence in the prior art that ALD is a *conformal process*. If layer 64 can not make its way to be evenly conformally deposited inside the trench as in Fig. 2E, then the first insulating layer would have problems with being conformally deposited by any method:

Perhaps applicant has omitted details of modifying an ALD process to perform a controlled selective sidewall deposition of layer 64 as seen in Fig 2E. Perhaps applicant has omitted disclosure of a sacrificial layer in forming layer 64. Perhaps applicant has omitted disclosure of masking in forming layer 64.

Correction and/or explanation are required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 12 and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Wei (US 6,025,245).

Regarding claim 12, the Wei reference discloses "A method of manufacturing a trench capacitor" [title] comprising: defining a semiconductor substrate (i.e. 201 is defined as a "silicon substrate" wherein the "silicon substrate" is of course a "semiconductor substrate"), forming a trench with a lower region and an upper region in the semiconductor substrate, the trench further having sidewalls (seen in the cover figure, but don't all trenches have an upper region, a lower region and sidewalls?);

forming a first conductive region around the lower region (i.e. plate 207); forming a collar oxide on and into (see 205 in Fig. 3) the sidewalls at an intermediate region (i.e. between the top and bottom of the trench 200); forming a dielectric layer (nitride 208) along the sidewalls of the trench 200 up to a level above the collar oxide (i.e. dielectric 208 is at a level "above" collar 205 in Fig. 6).

Regarding claim 17, Fig. 6 shows a structure that anticipates:

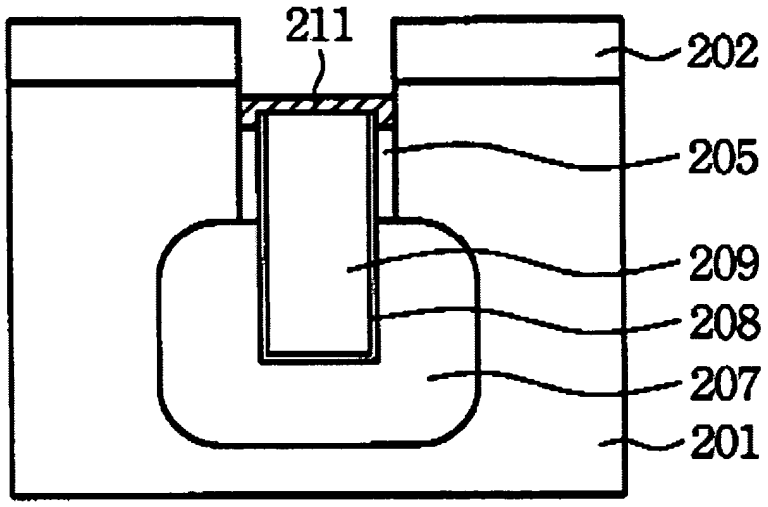

FIG.6

17. A trench capacitor comprising:
a trench (200 in Fig. 2) formed into a semiconductor substrate including a lower region and an upper region (e.g. 211, 208 and 209 are in the trench into substrate 201, the trench inherently having upper top and lower bottom regions), a first conductive region formed around the lower region of the trench (plate 207), a collar oxide (205) formed on and into ("into" per Fig. 3) sidewalls of the trench at an intermediate region between the lower region and the upper region (i.e. anywhere between top and bottom of the trench being an "intermediate region"), a dielectric layer (208) formed along the sidewalls of the trench up to a level above the collar oxide (205); and a second conductive region (209) formed up to the level (i.e. "up to" *and* "above").

Regarding claim 18, a "third conductive region" (i.e. 211) is formed over the "second conductive region" (i.e. 209).

Regarding claim 19, Wei discloses both nitride-oxide and oxide-nitride-oxide: Wei points out, "as is known in the art of DRAM capacitor fabrication, the nitride-oxide film is reliable over a silicon surface, and is typically used as a capacitor insulator," yet also recognizes the alternative use of an oxide-nitride-oxide as claimed [col. 3, lines 51-62].

Regarding claim 20, the dielectric layer (i.e. 208 in Fig. 6) is formed "up to a top level of the collar oxide (205)," because 208 is "up to a top level of 205" and extending a little further to also be "above" as well, as is claimed in claim 17 from which claim 20 depends (see item 1 above).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The examiner cites US 2003/0123216 A1 and EP 0 980 100 A for disclosing trench capacitor structures with a collar having a dielectric on sidewalls up to a level above collar oxide, yet the examiner refrains from making redundant prior art rejections, for increased clarity.

Furthermore, the '216 document reinforces the questions of enablement set forth in this Office Action (see [0006] wherein the first insulating layer of applicant's claimed invention could not deposit if the second layer naturally deposits to be separated from the first as in Fig. 6E under question).

US 5,142,438 is cited as a good background of the difference between types of DRAM capacitors, such as trench capacitors, with their common problems and solutions; for example, '438 indicates pending claim 19's "ONO" is used in "most contemporary (i.e. 1991) DRAM cells" [col. 2, lines 52-55].

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EVAN PERT
PRIMARY EXAMINER

ETP
May 5, 2005